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09/691,634	10/18/2000	Shervin Moloudi	39388/CAG/B600	7052

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EXAMINER	
MILORD, MARCEAU	
ART UNIT	PAPER NUMBER
2682	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,634	MOLOUDI ET AL.	
	Examiner	Art Unit	
	Marceau Milord	2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-41* is/are allowed.

6)☒ Claim(s) *1-12,15-18,20,21,42-53,56-76 and 79-94* is/are rejected.

7)☒ Claim(s) *13,14,54,55,77,78 and 95* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-12, 15-18, 20-21, 42-53, 56-76, 79-94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US Patent No 6194962 B1) in view of Murphy (US Patent No6157257).

Regarding claim 1, Chen discloses an amplifier (figs. 3-4), comprising: a plurality of differential pairs (MP1 and MP2) coupled through a differential output, each differential pair (MP1 and MP2) having a current control input (col. 2, lines 41-61; col. 3, lines 38-57; col. 5, lines 3-32; col. 3, line 58- col. 4, line 67; col. 6, line 45- col. 7, line 22).

However, Chen does not specifically disclose a switch coupled to the current control input of one of the differential pairs to selectively switch said one of the differential pairs in or out of the amplifier.

On the other hand, Murphy, from the same field of endeavor, discloses a folding amplifier in which a single tail current is used to service all differentially coupled transistor pairs in the amplifier. The input signal applied to each differential pair of transistors is used to drive a switch which controls the tail current to that specific differential pair. When a differential pair is fully switched in either direction, the associated tail current switch is open (col. 3, lines 18-34). In addition, Each differential pair includes a first transistor having a gate electrode coupled to one side of a differential input, and a second transistor having a gate electrode coupled to the other side of the differential input. The input signal V.sub.n P/V.sub.n N to a given differential pair is used to switch the tail current IT to that specific differential pair, and thus determines the amount of current allowed into that pair. When a differential pair is fully switched in either direction, the associated switch Sn is open (col. 5, lines 16-53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Murphy to the system of Chen in order to increase the common mode input voltage range and the voltage swing capability of this amplifier.

Regarding claim 2, Chen as modified discloses an amplifier (figs. 3-4), wherein the differential pairs each comprises first and second transistors coupled together through a common node, the common node comprising the current control input (col. 3, lines 39-67; col. 4, line 65-col. 5, line 45).

Regarding claim 3, Chen as modified discloses an amplifier (figs. 3-4), wherein the transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) each comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 4, Chen as modified discloses an amplifier (figs. 3-4); wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each differential pair each comprises a source coupled to its respective common node (col. 4, line 65- col. 5, line 64).

Regarding claim 5, Chen as modified discloses an amplifier (figs. 3-4), wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each of the differential pairs each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input (col. 5, lines 3- 42; col. 6, lines 1-31).

Regarding claim 6, Chen as modified discloses an amplifier (figs. 3-4), wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form the differential output (col. 5, lines 3-45; col. 6, lines 1-31).

Regarding claim 7, Chen as modified discloses an amplifier (figs. 3-4), wherein the current switch (32 of fig. 3) comprises a transistor (MP1 of fig. 3; col 5, lines 1- 37).

Regarding claim 8, Chen as modified discloses an amplifier (figs. 3-4), wherein the transistor comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 9, Chen as modified discloses an amplifier (figs. 3-4), wherein the transistor comprises a drain coupled to its respective current control input (col. 5, lines 3-37; col. 6, lines 1-56).

Regarding claim 10, Chen as modified discloses an amplifier (figs. 3-4); wherein the current switch (32 of fig. 3) comprises a current source (30 of fig. 3) having a switch control input (32 of fig. 3; col. 4, lines 45-67; col. 5, lines 3- 45).

Regarding claim 11, Chen as modified discloses an amplifier (figs. 3-4), further comprising a bias circuit coupled to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 12, Chen as modified discloses an amplifier (figs. 3-4), wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 15, Chen as modified discloses an amplifier (figs. 3-4), wherein the current source comprises a field effect transistor having a gate comprising the switch control input (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 16, Chen as modified discloses an amplifier (figs. 3-4), further comprising a matching circuit coupled to the common differential output (col. 3, line 47- col. 4, line 32).

Regarding claim 17, Chen as modified discloses an amplifier (figs. 3-4), wherein the matching circuit converts a differential current from the common differential output to a single-ended current (col. 3, line 47- col. 4, line 48).

Regarding claim 18, Chen as modified discloses an amplifier (figs. 3-4), wherein the matching circuit provides an impedance transformation which is independent of whether said one of the differential pairs is switched in or out of the amplifier (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 20, Chen as modified discloses an amplifier (figs. 3-4), wherein the differential pairs are further coupled together through a common differential input, the amplifier further comprising an input stage coupled to the common differential input (col. 5, lines 3- 42; col. 6, lines 1-31).

Regarding claim 21, Chen as modified discloses an amplifier (figs. 3-4), further comprising a plurality of current switches each coupled to the current control input for a different one of the differential pairs to selectively switch its respective differential pair in or out of the amplifier (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 42, Chen discloses an amplifier (figs. 3-4), comprising:
a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input (col. 2, lines 41-61; col. 3, lines 38-57; col. 5, lines 3-32; col. 3, line 58- col. 4, line 67; col. 6, line 45- col. 7, line 22).

However, Chen does not specifically disclose a switch coupled to the current control input of one of the amplifying stages.

On the other hand, Murphy, from the same field of endeavor, discloses a folding amplifier in which a single tail current is used to service all differentially coupled transistor pairs in the amplifier. The input signal applied to each differential pair of transistors is used to drive a switch which controls the tail current to that specific differential pair. When a differential pair is fully switched in either direction, the associated tail current switch is open (col. 3, lines 18-34). In addition, Each differential pair includes a first transistor having a gate electrode coupled to one side of a differential input, and a second transistor having a gate electrode coupled to the other side of the differential input. The input signal V.sub.n P/V.sub.n N to a given differential

pair is used to switch the tail current IT to that specific differential pair, and thus determines the amount of current allowed into that pair. When a differential pair is fully switched in either direction, the associated switch Sn is open (col. 5, lines 16-53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Murphy to the system of Chen in order to increase the common mode input voltage range and the voltage swing capability of this amplifier.

Regarding claim 43, Chen as modified discloses an amplifier (figs. 3-4), wherein the amplifying stages each comprises first and second transistors coupled together through a common node, the common node comprising the current control input (col. 3, lines 39-67; col. 4, line 65- col. 5, line 45).

Regarding claim 44, Chen as modified discloses an amplifier (figs. 3-4), wherein the transistors each comprise a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 45, Chen as modified discloses an amplifier (figs. 3-4); wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each amplifying stage comprises a source coupled to its respective common node (col. 4, line 65- col. 5, line 64).

Regarding claim 46, Chen as modified discloses an amplifier (figs. 3-4), wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input (col. 4, line 65- col. 5, line 64).

Regarding claim 47, Chen as modified discloses an amplifier (figs. 3-4), wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each of the differential

pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output (col. 5, lines 3-45; col. 6, lines 1-31).

Regarding claim 48, Chen as modified discloses an amplifier (figs. 3-4), wherein the current switch comprises a transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 49, Chen as modified discloses an amplifier (figs. 3-4), wherein the transistor comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 50, Chen as modified discloses an amplifier (figs. 3-4), wherein the transistor comprises a drain coupled to its respective current control input (col. 5, lines 3-37; col. 6, lines 1-56).

Regarding claim 51, Chen as modified discloses an amplifier (figs. 3-4); wherein the current switch comprises a current source having a switch control input (32 of fig. 3; col. 4, lines 45-67; col. 5, lines 3- 45).

Regarding claim 52, Chen as modified discloses an amplifier (figs. 3-4); further comprising a bias circuit coupled to the switch control inputs (col. 3, line 47- col. 4, line 19).

Regarding claim 53, Chen as modified discloses an amplifier (figs. 3-4), wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 56, Chen as modified discloses an amplifier (figs. 3-4), wherein the current source comprises a field effect transistor having a gate comprising the switch control input (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 57, Chen as modified discloses an amplifier (figs. 3-4), further comprising a matching circuit coupled to the differential output (col. 3, line 47- col. 4, line 32).

Regarding claim 58, Chen as modified discloses an amplifier (figs. 3-4), wherein the matching circuit converts a differential current from the differential output to a single-ended current (col. 3, line 47- col. 4, line 48).

Regarding claim 59, Chen as modified discloses an amplifier (figs. 3-4), wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 61, Chen as modified discloses an amplifier (figs. 3-4), wherein the amplifying stages are coupled together to form a differential input, the amplifier further comprising an input stage coupled to the differential input (col. 5, lines 3- 42; col. 6, lines 1-31).

Regarding claim 62, Chen as modified discloses an amplifier (figs. 3-4), further comprising a plurality of current switches each coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 63, Chen as modified discloses an amplifier (figs. 3-4), comprising a digitally programmable power level and a matching circuit, which is substantially independent of the programmed power level (col. 2, lines 41-61; col. 3, lines 38-57; col. 5, lines 3-32).

Regarding claim 64, Chen as modified discloses an amplifier (figs. 3-4), wherein the amplifier comprises CMOS (col. 6, lines 5-36).

Regarding claim 65, Chen as modified discloses an amplifier (figs. 3-4), comprising a plurality of amplifying stages coupled together, each of the amplifying stages having a current

control input, and a plurality of current switches to digitally program the power level of the amplifier, the current switches each being coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 66, Chen as modified discloses an amplifier (figs. 3-4), wherein the amplifying stages each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input (col. 3, lines 39-67; col. 4, line 65- col. 5, line 45).

Regarding claim 67, Chen as modified discloses an amplifier (figs. 3-4), wherein the transistors each comprise a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 68, Chen discloses an amplifier (figs. 3-4); wherein the first and second transistors in each amplifying stage comprises a source coupled to its respective common node (col. 4, line 65- col. 5, line 64).

Regarding claim 69, Chen as modified discloses an amplifier (figs. 3-4), wherein the first and second transistors in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input (col. 4, line 65- col. 5, line 64).

Regarding claim 70, Chen as modified discloses an amplifier (figs. 3-4), wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output (col. 5, lines 3-45; col. 6, lines 1-31).

Regarding claim 71, Chen as modified discloses an amplifier (figs. 3-4), wherein the current switches each comprise a transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 72, Chen as modified discloses an amplifier (figs. 3-4), wherein the transistors each comprise a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 73, Chen as modified discloses an amplifier (figs. 3-4 wherein the transistors each comprises a drain coupled to its respective current control input (col. 5, lines 3-37; col. 6, lines 1-56).

Regarding claim 74, Chen as modified discloses an amplifier (figs. 3-4), wherein the current switches each comprise a current source having a switch control input (32 of fig. 3; col. 4, lines 45-67; col. 5, lines 3- 45).

Regarding claim 75, Chen as modified discloses an amplifier (figs. 3-4) comprising a plurality of bias circuits each coupled to a different one of the switch control inputs (col. 3, line 47- col. 4, line 19).

Regarding claim 76, Chen as modified discloses an amplifier (figs. 3-4), wherein the bias circuits each generates a bias current which is substantially independent of temperature, the bias current being applied to its respective switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 79, Chen as modified discloses an amplifier (figs. 3-4); wherein the current sources each comprise a field effect transistor having a gate comprising the switch control input (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 80, Chen discloses an amplifier (figs. 3-4), comprising:
a plurality of amplifying stages coupled together (col. 2, lines 41-61; col. 3, lines 38-57; col. 5, lines 3-32); and matching means for matching a load coupled to an output of the amplifier, the

matching means being substantially independent of the programmed power (col. 6, line 45- col. 7, line 22).

However, Chen does not specifically disclose the step of switching means for switching one of the amplifying stages in or out of the amplifier to program power of the amplifier.

On the other hand, Murphy, from the same field of endeavor, discloses a folding amplifier in which a single tail current is used to service all differentially coupled transistor pairs in the amplifier. The input signal applied to each differential pair of transistors is used to drive a switch which controls the tail current to that specific differential pair. When a differential pair is fully switched in either direction, the associated tail current switch is open (col. 3, lines 18-34). In addition, Each differential pair includes a first transistor having a gate electrode coupled to one side of a differential input, and a second transistor having a gate electrode coupled to the other side of the differential input. The input signal V.sub.n P/V.sub.n N to a given differential pair is used to switch the tail current IT to that specific differential pair, and thus determines the amount of current allowed into that pair. When a differential pair is fully switched in either direction, the associated switch Sn is open (col. 5, lines 16-53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Murphy to the system of Chen in order to increase the common mode input voltage range and the voltage swing capability of this amplifier.

Regarding claim 81, Chen as modified discloses an amplifier (figs. 3-4), wherein each of said one of the amplifying stage comprises first and second transistors coupled together through a common a node, the common node comprising the current control input (col. 3, lines 39-67; col. 4, line 65- col. 5, line 45).

Regarding claim 82 Chen as modified discloses an amplifier (figs. 3-4), wherein the transistors each comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 83, Chen as modified discloses an amplifier (figs. 3-4), wherein the first and second transistors each comprises a source coupled to its respective common node (col. 4, line 65- col. 5, line 64).

Regarding claim 84, Chen as modified discloses an amplifier (figs. 3-4), wherein the amplifying stages each comprises first and second field effect transistors each having a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input (col. 4, line 65- col. 5, line 64).

Regarding claim 85, Chen as modified discloses an amplifier (figs. 3-4), wherein the amplifying stages each comprises first and second field effect transistors each having a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output (col. 5, lines 3-45; col. 6, lines 1-31).

Regarding claim 86, Chen as modified discloses an amplifier (figs. 3-4), wherein the switching means comprises a transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 87, Chen as modified discloses an amplifier (figs. 3-4), wherein the transistor comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 88, Chen as modified discloses an amplifier (figs. 3-4); wherein the transistor comprises a drain coupled to said one of the amplifying stages (col. 5, lines 3-37; col. 6, lines 1-56).

Regarding claim 89, Chen as modified discloses an amplifier (figs. 3-4); wherein the switching means comprises a current source having a switch control input (32 of fig. 3; col. 4, lines 45-67; col. 5, lines 3- 45).

Regarding claim 90, Chen as modified discloses an amplifier (figs. 3-4), further comprising a bias circuit coupled to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 91, Chen as modified discloses an amplifier (figs. 3-4), wherein the bias circuit comprises means for generating a bias current which is substantially independent of temperature, the bias current being applied to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 92, Chen as modified discloses an amplifier (figs. 3-4), wherein the bias circuit comprises means for generating a first bias current exhibiting a positive temperature coefficient, means for generating a second bias current exhibiting a negative temperature coefficient, and means for summing the first and second bias currents, the summed first and second bias currents being applied to the switch control input (col. 4, lines 3-67; col. 5, lines 3-45; col. 7, lines 23- 67).

Regarding claim 93, Chen as modified discloses an amplifier (figs. 3-4), wherein the summer comprises a cascode current mirror (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 94, Chen as modified discloses an amplifier (figs. 3-4), wherein the matching means comprises means for converting a differential current generated by the amplifier stage to a single-ended current, the single ended current being coupled to the amplifier output (col. 3, line 47- col. 4, line 48).

2. Claims 19, 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US Patent No 6194962 B1) in view of Murphy (US Patent No6157257) as applied to claims 1, 22, 42 above, and further in view of Ciccarelli et al (US Patent No 6175279 B1).

Regarding claims 19 and 60, Chen and Murphy disclose everything claimed as explained above except an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

However, Ciccarelli et al discloses an amplifier having an adjustable current source, which can be controlled to provide the requisite level of performance at reduced current consumption. The current source is then designed to provide adjustable bias current for the amplifier. Furthermore, Ciccarelli shows in figure 5A, a capacitor 1514 that connects to analog ground and the other end of inductor 1516 connects to one end of resistors 1518 and 1520 and the base of transistor 1540. Capacitor 1514 and inductor 1516 provide noise matching. Inductors 1516 and 1532 also provide matching of the LNA input and output, respectively. Inductor 1542 also provides degeneration of the emitter impedance to improve linearity (col. 4, line 35- col. 5, line 13; col. 9, line 25-col. 10, line 35). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ciccarelli to the modified system of Murphy and Chen in order to adjust the current source based on the measured and required performance of the amplifier.

Allowable Subject Matter

3. Claims 22-41 are allowed.

Allowable Subject Matter

4. Claims 13-14, 54-55, 77-78, 95 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments with respect to claims 1-12, 15-18, 20-21, 42-53, 56-76, 79-94 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 571-272-7853. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, To H. Doris can be reached on 571-272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARCEAU MILORD Marceau Milord

Primary Examiner

Art Unit 2682